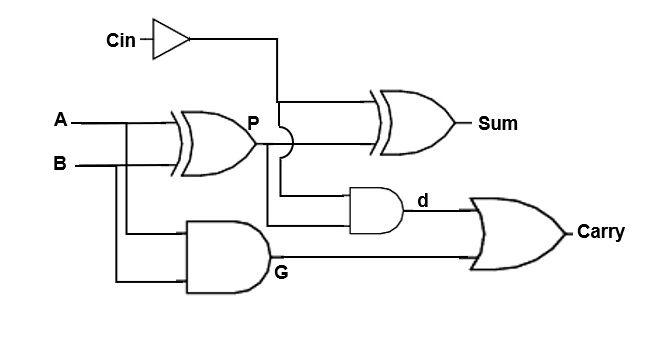
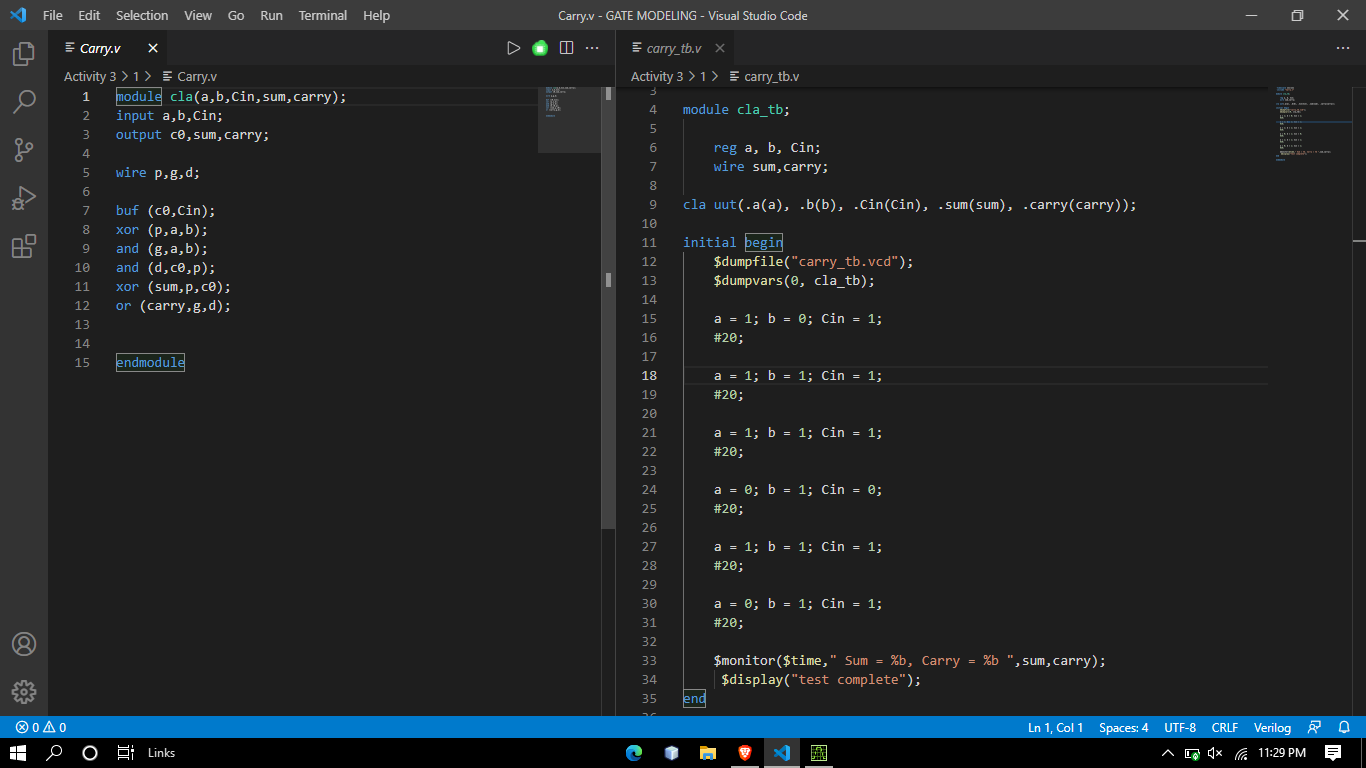
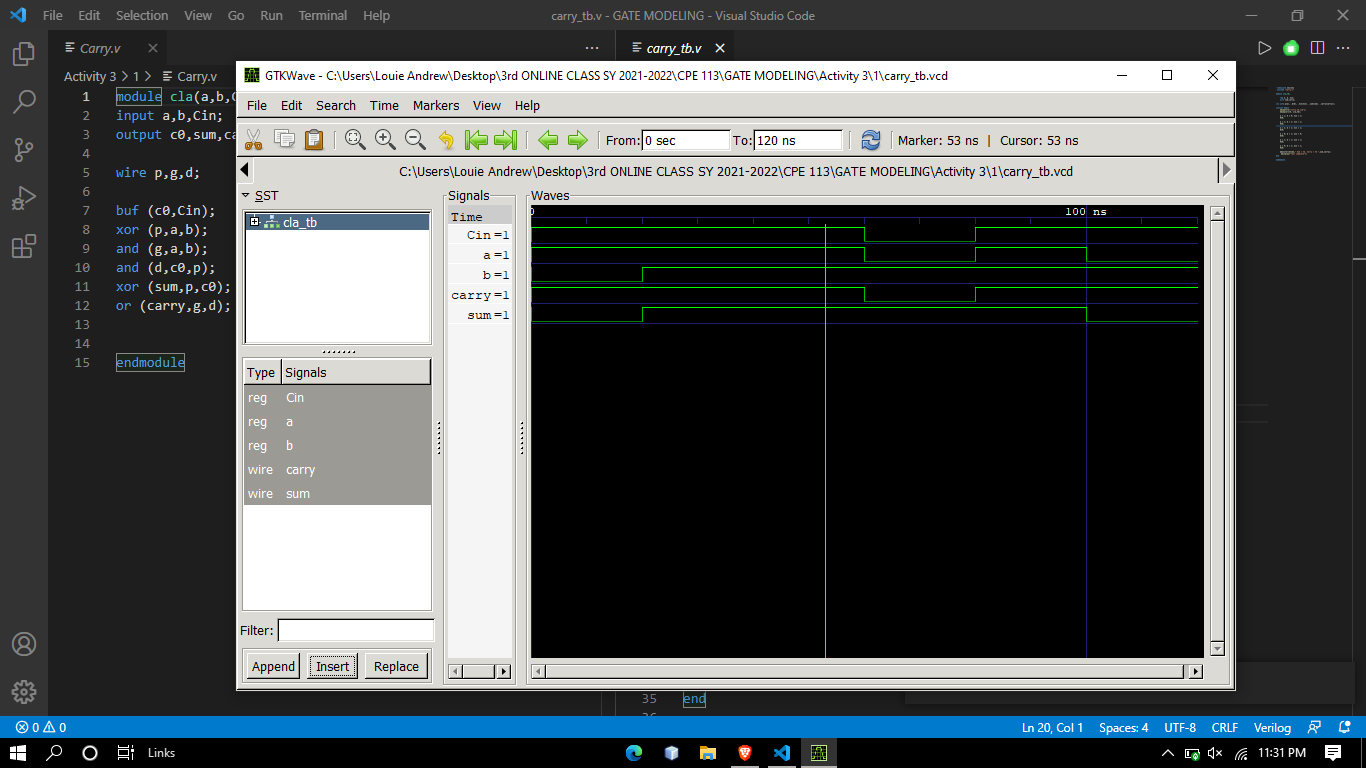
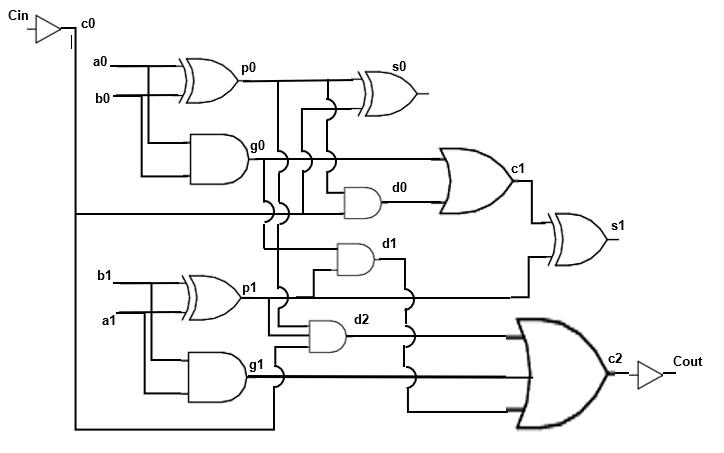
Carry Look Ahead Adder

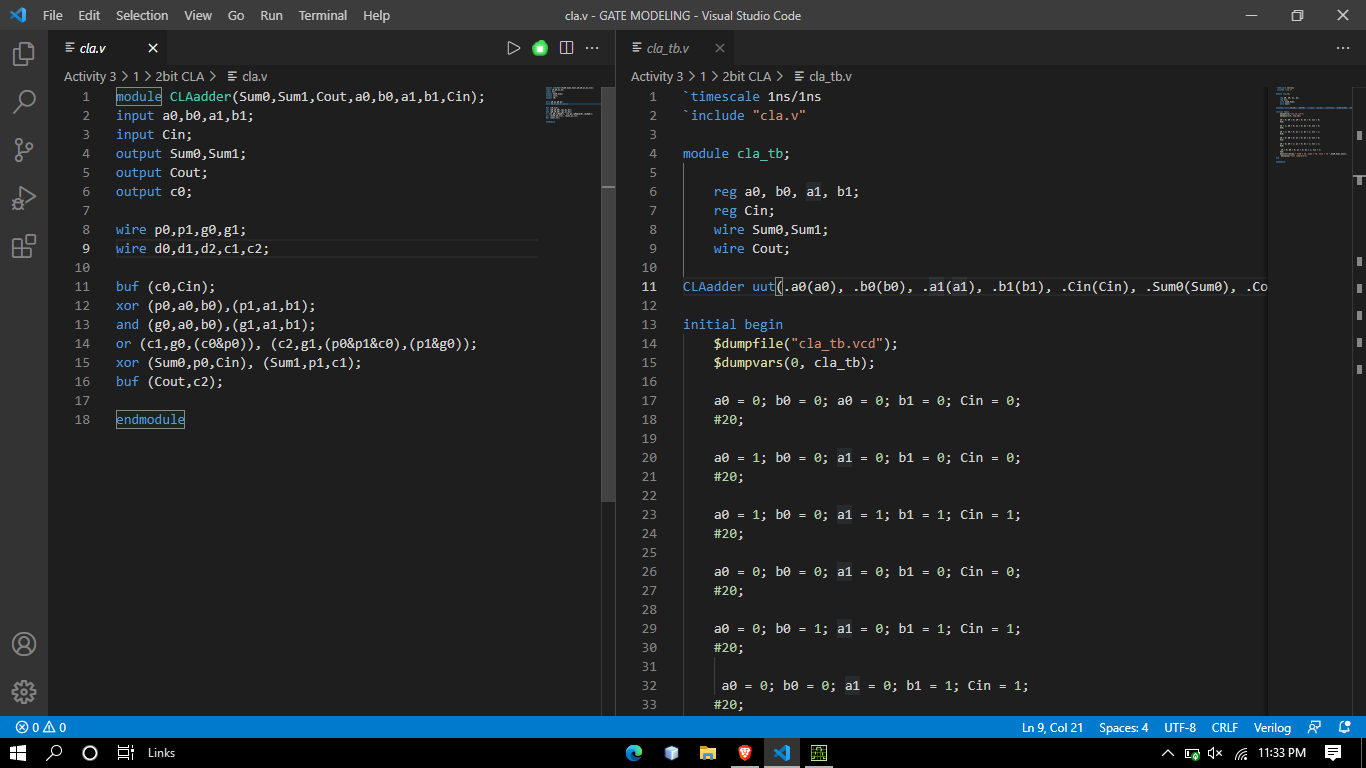


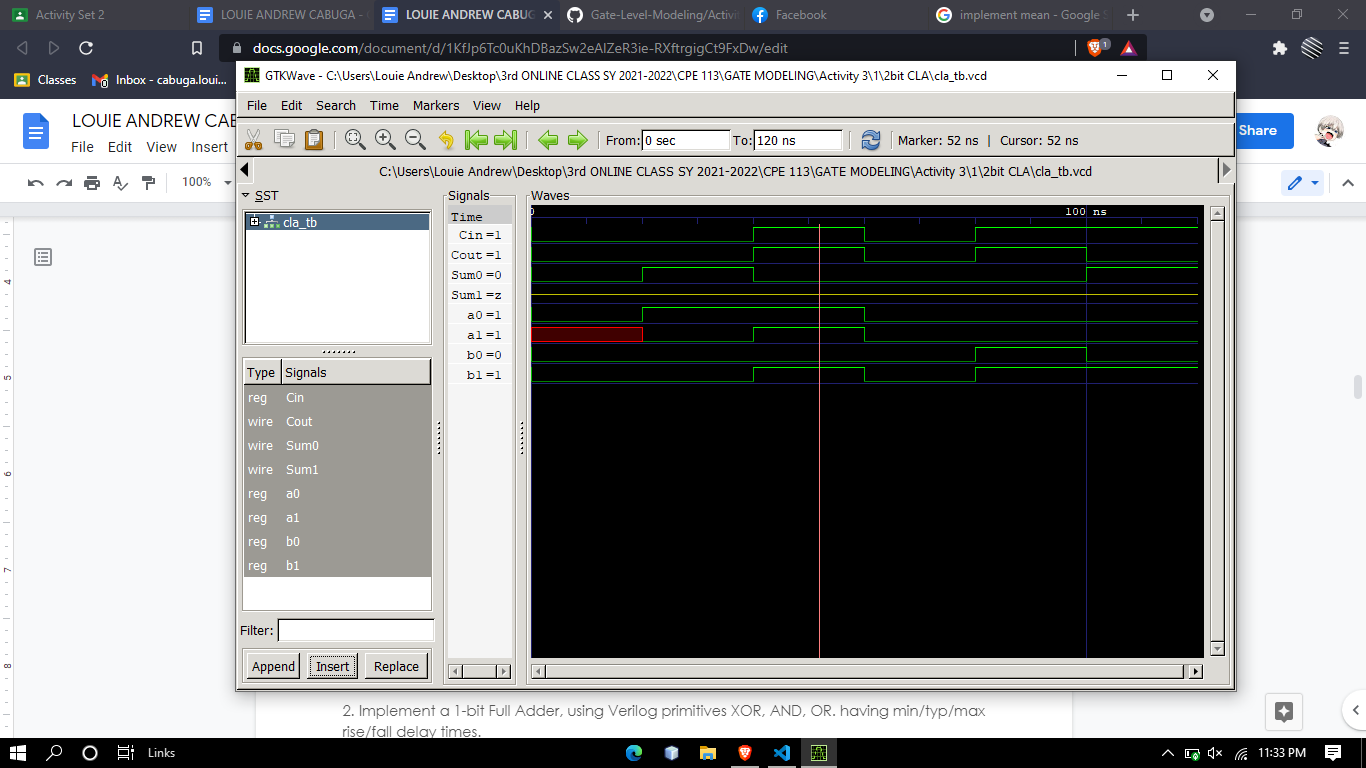
[](https://github.com/Origin101/Gate-Level-Modeling/tree/main/Activity%203/1)



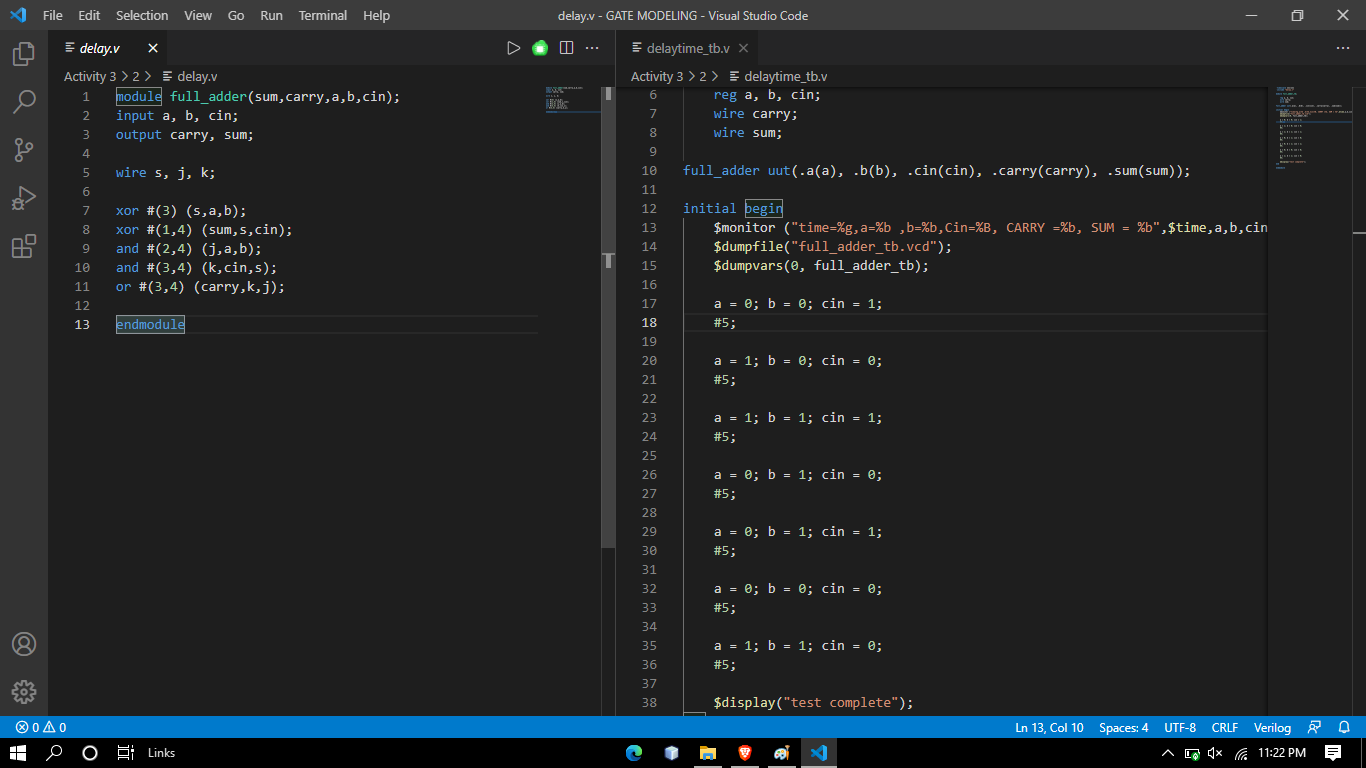
2 bits Carry Look Ahead adder

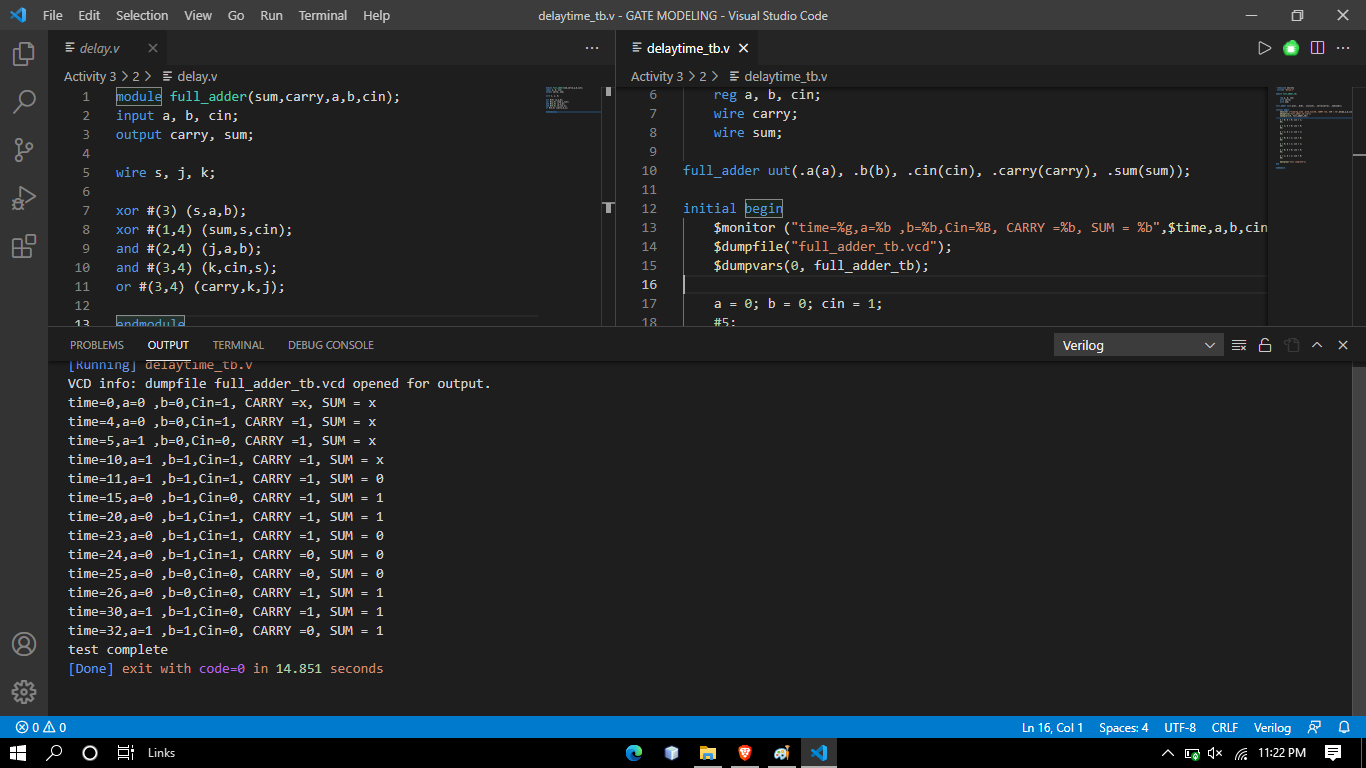


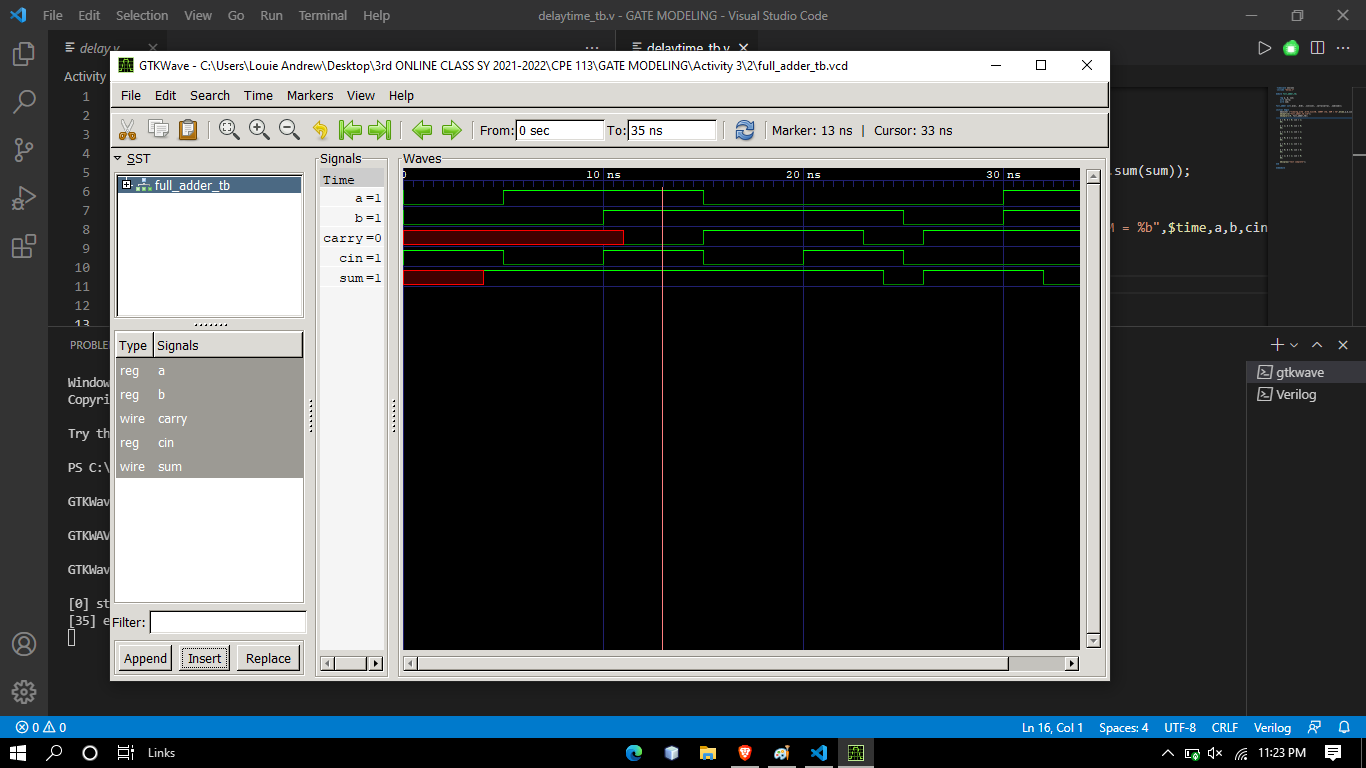




2. Implement a 1-bit Full Adder, using Verilog primitives XOR, AND, OR. having min/typ/max rise/fall delay times.







3. Design a Byte Comparator, using an array of 2-input XOR primitives, 8-input OR primitive and NOTIF1 buffer, enabled by an input signal.

